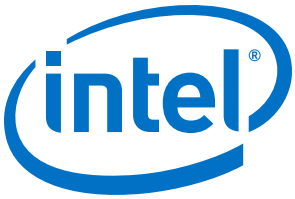

# External Memory Interfaces Intel® Arria® 10 FPGA IP User Guide

Updated for Intel® Quartus® Prime Design Suite: **19.3**

IP Version: **19.1.0**

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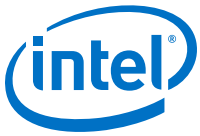

### Table 202. Group: Board / Intersymbol Interference/Crosstalk

| Display Name | Description |
|---|---|
| **Use default ISI/crosstalk values** | You can enable this option to use default intersymbol interference and crosstalk values for your topology. Note that the default values are not optimized for your board. *For optimal signal integrity, it is recommended that you do not enable this parameter, but instead perform I/O simulation using IBIS models and Hyperlynx*, and manually enter values based on your simulation results, instead of using the default values.* (Identifier: BOARD_DDR3_USE_DEFAULT_ISI_VALUES) |
| **Address and command ISI/crosstalk** | The address and command window reduction due to ISI and crosstalk effects. The number to be entered is the **total loss of margin on both the setup and hold sides (measured loss on the setup side + measured loss on the hold side)**. *Refer to the EMIF Simulation Guidance wiki page for additional information.* (Identifier: BOARD_DDR3_USER_AC_ISI_NS) |
| **Read DQS/DQS# ISI/crosstalk** | The reduction of the read data window due to ISI and crosstalk effects on the DQS/DQS# signal when driven by the memory device during a read. The number to be entered is the **total loss of margin on the setup and hold sides (measured loss on the setup side + measured loss on the hold side)**. *Refer to the EMIF Simulation Guidance wiki page for additional information.* (Identifier: BOARD_DDR3_USER_RCLK_ISI_NS) |
| **Read DQ ISI/crosstalk** | The reduction of the read data window due to ISI and crosstalk effects on the DQ signal when driven by the memory device during a read. The number to be entered is the **total loss of margin on the setup and hold side (measured loss on the setup side + measured loss on the hold side)**. *Refer to the EMIF Simulation Guidance wiki page for additional information.* (Identifier: BOARD_DDR3_USER_RDATA_ISI_NS) |
| **Write DQS/DQS# ISI/crosstalk** | The reduction of the write data window due to ISI and crosstalk effects on the DQS/DQS# signal when driven by the FPGA during a write. The number to be entered is the **total loss of margin on the setup and hold sides (measured loss on the setup side + measured loss on the hold side)**. *Refer to the EMIF Simulation Guidance wiki page for additional information.* (Identifier: BOARD_DDR3_USER_WCLK_ISI_NS) |
| **Write DQ ISI/crosstalk** | The reduction of the write data window due to ISI and crosstalk effects on the DQ signal when driven by the FPGA during a write. The number to be entered is the **total loss of margin on the setup and hold sides (measured loss on the setup side + measured loss on the hold side)**. *Refer to the EMIF Simulation Guidance wiki page for additional information.* (Identifier: BOARD_DDR3_USER_WDATA_ISI_NS) |

### Table 203. Group: Board / Board and Package Skews

| Display Name | Description |
|---|---|
| **Package deskewed with board layout (DQS group)** | Enable this parameter if you are compensating for package skew on the DQ, DQS, and DM buses in the board layout. **Include package skew in calculating the following board skew parameters.** (Identifier: BOARD_DDR3_IS_SKEW_WITHIN_DQS_DESKEWED) |
| **Maximum board skew within DQS group** | The largest skew between all DQ and DM pins in a DQS group. This value affects the read capture and write margins. (Identifier: BOARD_DDR3_BRD_SKEW_WITHIN_DQS_NS) |
| **Maximum system skew within DQS group** | The largest skew between all DQ and DM pins in a DQS group. Enter combined board and package skew. This value affects the read capture and write margins. (Identifier: BOARD_DDR3_PKG_BRD_SKEW_WITHIN_DQS_NS) |
| **Package deskewed with board layout (address/command bus)** | Enable this parameter if you are compensating for package skew on the address, command, control, and memory clock buses in the board layout. **Include package skew in calculating the following board skew parameters.** (Identifier: BOARD_DDR3_IS_SKEW_WITHIN_AC_DESKEWED) |

***continued...***